In the Claims:

Please amend the claims as follows.

1. (Currently Amended) A method of creating a simulation history for a selected simulation session range ~~a value change dump (VCD) file~~ for a hardware modeled design on demand, comprising steps:

selecting a simulation session range ~~which begins at a simulation time t0 and ends at a simulation time t3~~;

selecting a simulation target range, wherein the simulation target range is within the simulation session range ~~which begins at a simulation time t1 and ends at a simulation time t2, wherein the simulation time t1 is greater than or equal to simulation time t0 and simulation time t2 is less than or equal to simulation time t3~~; and

generating a value change dump (VCD) ~~VCD~~ file by dumping state information from the hardware ~~of the~~ modeled design for the selected simulation target range ~~; and~~

~~accessing the VCD file directly from simulation time t1 to debug the modeled design~~.

2. (Currently Amended) The method of claim 1, further comprising steps:

accessing the VCD file directly from the beginning of the simulation target range to debug the modeled design;

providing primary inputs to the hardware modeled design for evaluation; and

recording a simulation history for the simulation session range.

3. (Currently Amended) The method of claim ~~2~~ 21, further comprising steps:

processing the simulation history; and

evaluating in the modeled design the processed simulation history from simulation time t0 to simulation time t2.

4. (Original) The method of claim 3, wherein the step of generating the VCD file further comprises:

generating evaluated results from the modeled design based on the processed simulation history; and

saving the evaluated results during the simulation target range into the VCD file.

5. (Original) The method of claim 4, wherein the step of recording further comprises steps:

compressing the primary inputs; and

recording the compressed primary inputs as the simulation history.

6. (Original) The method of claim 4, wherein the processing step further comprises:

decompressing the compressed primary inputs; and

providing the decompressed primary inputs as the processed simulation history to the modeled design for evaluation.

7. (Original) The method of claim 4, wherein the recording step includes the step of:

recording the primary inputs as the simulation history.

8. (Currently Amended) The method of claim ~~1~~ 21, further comprising steps:

saving state information of the modeled design at simulation time t0 in a first file; and

saving state information of the modeled design at simulation time t3 in a second file.

9. (Original) An electronic design automation system for verifying a user design, comprising:

a computing system including a central processing unit and memory for modeling the user design in software;

an internal bus system coupled to the computing system;

reconfigurable hardware logic coupled to the internal bus system and for modeling at least a portion of the user design in hardware;

control logic coupled to the internal bus system for controlling the delivery of data between the reconfigurable hardware logic and the computing system; and

VCD on-demand logic for recording a simulation history for a selected simulation session range and dumping state information from the hardware model into a VCD file for a selected simulation target range, where the simulation target range is within the simulation session range.

10. (Original) The electronic design automation system of claim 9, wherein the VCD on-demand logic further comprises:

first range selection logic for selecting a simulation session range which begins at a simulation time t0 and ends at a simulation time t3;

second range selection logic for selecting a simulation target range which begins at a simulation time t1 and ends at a simulation time t2, wherein the simulation time t1 is greater than or equal to simulation time t0 and simulation time t2 is less than or equal to simulation time t3;

dump logic for generating a VCD file of the hardware-modeled design for the selected simulation target range; and

access logic for accessing the VCD file directly from simulation time t1 to debug the user design.

11. (Original) The electronic design automation system of claim 10, wherein the VCD on-demand logic further comprises:

test bench process for providing primary inputs to the hardware-modeled design for evaluation; and

recording logic in the computing system for recording a simulation history for the simulation session range.

12. (Original) The electronic design automation system of claim 11, wherein the VCD on-demand logic further comprises:

process logic in the computing system for processing the simulation history; and

evaluation logic in the reconfigurable hardware logic for evaluating in the hardware-modeled design the processed simulation history from simulation time t0 to simulation time t2.

13. (Original) The electronic design automation system of claim 12, wherein the dump logic dumps the evaluated results from the hardware-modeled design based on the processed simulation history during the simulation target range into the VCD file.

14. (Original) The electronic design automation system of claim 13, wherein the recording logic further comprises:

compression logic for compressing the primary inputs; and

write logic for writing the compressed primary inputs as the simulation history.

15. (Original) The electronic design automation system of claim 14, wherein the process logic further comprises:

decompression logic for decompressing the compressed primary inputs; and

data transfer logic for delivering the decompressed primary inputs as the processed simulation history to the hardware-modeled design for evaluation.

16. (Original) The electronic design automation system of claim 13, wherein the recording logic further comprises:

write logic for writing the primary inputs as the simulation history.

17. (Original) The electronic design automation system of claim 9, further comprising:

state save logic for saving state information of the hardware-modeled design at simulation time t0 in a first file and saving state information of the hardware-modeled design at simulation time t3 in a second file.

18. (Currently Amended) A VCD on-demand system for providing evaluated information for a selected simulation target range of simulation times, the evaluation occurring in a hardware model ~~modeled design~~, comprising:

first logic for selecting a simulation session range ~~which begins at a simulation time t0 and ends at a simulation time t3~~;

second logic selecting a simulation target range, wherein the simulation target range is within the simulation session range ~~which begins at a simulation time t1 and ends at a simulation time t2, wherein the simulation time t1 is greater than or equal to simulation time t0 and simulation time t2 is less than or equal to simulation time t3~~; and

generation logic for generating a VCD file of the evaluated information for the selected simulation target range by dumping state information from the hardware model ~~; and~~

~~access logic for accessing the VCD file directly from simulation time t1 to debug the modeled design~~.

19. (Currently Amended) The VCD on-demand system of claim 18, further comprising:

access logic for accessing the VCD file directly from the beginning of the simulation target range to debug the modeled design;

compression logic for receiving and compressing primary input data for the duration of the simulation session range; and

decompression logic for decompressing the compressed primary input data and delivering the decompressed primary input data into the modeled design for evaluation.

20. (Original) The VCD on-demand system of claim 19, wherein the generation logic further comprises:

dump logic for dumping evaluated information to the VCD file, the evaluated information generated by the evaluation of the decompressed primary inputs by the modeled design.

21. (New) The method of claim 1, wherein the simulation session range begins at a simulation time t0 and ends at a simulation time t3, and the simulation target range begins at a simulation time t1 and ends at a simulation time t2, wherein the simulation time t1 is greater than or equal to simulation time t0 and simulation time t2 is less than or equal to simulation time t3.

22. (New) The system of claim 18, wherein the simulation session range begins at a simulation time t0 and ends at a simulation time t3, and the simulation target range begins at a simulation time t1 and ends at a simulation time t2, wherein the simulation time t1 is greater than or equal to simulation time t0 and simulation time t2 is less than or equal to simulation time t3.